REMARKS

The above amendments to the above-captioned application along with the following remarks are being submitted as a full and complete response to the Official Action dated January 21, 2004. In view of the above amendments and the following remarks, the Examiner is respectfully requested to give due reconsideration to this application, to indicate the allowability of the claims, and to pass this case to issue.

Status of the Claims

Claims 1-22 are under consideration in this application. Claims 1, 11, 19 and 21 are being amended, as set forth above, in order to more particularly define and distinctly claim Applicants' invention.

Additional Amendments

The claims are being amended to correct formal errors and/or to better disclose or describe the features of the present invention as claimed. Applicants hereby submit that no new matter is being introduced into the application through the submission of this response.

Allowed Subject Matters

Claims 13 and 14 would be allowed, if they are rewritten in independent form to include all of the limitations of the base claim and any intervening claims.

Prior Art Rejections

Claims 1, 2, 7-12 and 15-22 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Pat. No. 5,050,165 to Yoshioka et al. (hereinafter "Yoshioka") in view of U.S. Pat. No. 5,287,452 to Newman (hereinafter "Newman"), and claims 3-6 were rejected as being unpatentable over Yoshioka in view of Newman and further in view of U.S. Pat. No. 4,918,647 to Downey (hereinafter "Downey"). The prior art references of Glover et al. (4,763,332), and Sollars (6,081,880) were cited as being pertinent to the present application. These rejections have been carefully considered, but are most respectfully traversed.

The data processor 1 of the invention (e.g., Fig. 1), as now recited in claim 1, comprises: a central processing unit 2; a data transfer control circuit (e.g., a direct memory access controller DMAC and a data transfer controller DTC 3 in Fig. 4; p. 1, 1st paragraph) for controlling data transfers under control of said central processing unit 2; and a peripheral circuit (e.g. an analog-to-digital converter ADC 16 in Fig. 2) and a timer counter TMR 11; p. 1, 1st paragraph) for requesting data transfers and for inputting data from outside of the data processor, and said peripheral circuit including a plurality of input terminals (e.g., input channels AN0-AN7). The peripheral circuit ADC 16 (p. 22 last paragraph – p. 25) selects one of input terminals thereof, processes input data from the selected input terminal, requests the transfer of the processing result, and outputs identification information (CH2 ~ CH0) which indicates the identification of the selected input terminal. The data transfer control circuit DTC 3 includes a destination address register DAR which has low-order bits variable with said identification information outputted from said peripheral circuit ADC 16 (p. 31, 2nd paragraph).

Therefore, the peripheral circuit ADC 16 does not need to have data registers for storing the processing results of input data according to the number of input terminals. The low-order bits of a destination address register DAR are automatically updated based on the identification information from the peripheral circuit ADC 16 such that the number of the data transfer channels of the data transfer control circuit DTC 3 do not have to increase along with the number of the input channels of the peripheral circuit ADC 16 (p. 4, lines 11-25; p. 43, last paragraph to p. 44). The invention eliminates the need for internal transferring of processing/control data from a memory to a transfer control register each time the peripheral circuit ADC 16 requests data to be transferred to the data transfer controller DTC 3. Each of a plurality of peripheral circuits can output data transfer request with identification information according to the invention to avoid setting up as many data registers therein as in the prior art.

The invention, as now recited in claims 11, 19 and 21, is also directed to other embodiments of data processors, which are essentially the same as the one recited in claim 1, but phrased slightly differently.

None of the cited prior art references teaches or suggests such a "peripheral circuit ADC 16 outputting identification information (CH2 ~ CH0) which indicates the identification of the selected input terminal" and such a "data transfer control circuit DTC

3 with a destination address register DAR which has low-order bits variable with said identification information outputted from said peripheral circuit ADC 16" thereby reducing number of data registers in ADC 16 to be few than the number of input terminals of ADC 16 as recited in claim 1.

As admitted by the Examiner, Yoshioka does "*not teach low-order bits variable according to the identification information from a peripheral circuit* (p. 3, lines 7-8)." As such, Yoshioka fails to teach a peripheral circuit outputs identification information of its selected input terminal which is used to update the low-order bits of a destination address register DAR in a data transfer control circuit DTC.

Yoshioka merely connects a bridge circuit 3 to plural networks (1A,2A,1B in Fig. 1), and the bridge circuit 3 has many built-in circuit modules 11,12,31,32,33,51,52. The data or coded signals read from the look-up memory 52 are supplied to a decision circuit 33 through a bus 56, and the decision circuit 33 outputs a stop signal on a line 39 as the result of decision. When the stop signal appears on the line 39 during sending a message, the LAN controller 12 supplies the interrupt signal to the MPU 61. By adopting this control method, transfer is prohibited when a destination address and a source address are connected to the same network. Yoshioka's control method is essentially different from a data transfer control method of the invention.

Newman was relied upon by the Examiner to teach low-order bits variable according to the identification information from a peripheral circuit. Newman displays an image in a computer system in such a manner as to not interface with the access to a system memory by a CPU even during refresh or update operation to the display memory, and allows the display memory to be updated simultaneously with the system memory without requiring extra operation. Newman generates the horizontal and vertical addresses for the image being displayed, which essentially define column and row addresses, respectively, for the storage locations in the dual port memory 116. The horizontal address comprises a variable number of low order bits of the displacement virtual address value received from subtractor 232 (col. 7, lines 19-22) such that Newman processes low-order bits in a completely different way from the invention . Newman fails to teach any low-order bits of a destination address register DAR in a data transfer control circuit DTC to be updated based upon input of identification information of a selected input terminal of a peripheral circuit.

Downey was relied upon by the Examiner to teach some features recited in claims 3-6. However, Downey fails to compensate for the deficiencies of Yoshioka and Newman.

Although the invention applies the general identification mechanism of low-order bits, the invention applies the mechanism to identify the selected input terminal of a peripheral circuit which selected the input terminal to achieve unexpected results or properties, e.g., reducing number of data registers in ADC to be few than the number of input terminals of the ADC, or preventing the number of the data transfer channels of the data transfer control circuit DTC from increasing along with the number of the input channels of the ADC. The presence of these unexpected properties is evidence of nonobviousness. MPEP§716.02(a).

> "*Presence of a property not possessed by the prior art is evidence of nonobviousness. In re Papesch, 315 F.2d 381, 137 USPQ 43 (CCPA 1963) (rejection of claims to compound structurally similar to the prior art compound was reversed because claimed compound unexpectedly possessed anti-inflammatory properties not possessed by the prior art compound); Ex parte Thumm, 132 USPQ 66 (Bd. App. 1961) (Appellant showed that the claimed range of ethylene diamine was effective for the purpose of producing " 'regenerated cellulose consisting substantially entirely of skin' " whereas the prior art warned "this compound has 'practically no effect.' ").*

Although "[t]*he submission of evidence that a new product possesses unexpected properties does not necessarily require a conclusion that the claimed invention is nonobvious. In re Payne, 606 F.2d 303, 203 USPQ 245 (CCPA 1979). See the discussion of latent properties and additional advantages in MPEP § 2145*," the unexpected properties were unknown and non-inherent functions in view of Newman, since Newman does not inherently achieve the same results. In other words, these advantages would not flow naturally from following the teachings of Newman, since Newman fails to suggest any low-order bits of a destination address register DAR in a data transfer control circuit DTC to be updated based upon input of identification information of a selected input terminal of a peripheral circuit.

Applicants further contend that the mere fact that one of skill in the art could rearrange the low-order bits of Newman to meet the terms of the claims is not by itself sufficient to support a finding of obviousness. The prior art must provide a motivation or reason for one skilled in the art to provide the unexpected properties, such as reducing number of data registers in ADC to be few than the number of input terminals of the ADC, or preventing the number of the data transfer channels of the data transfer control circuit DTC from increasing along with the number of the input channels of the ADC, to make the necessary changes in the reference device. *Ex parte Chicago Rawhide Mfg. Co.*, 223 USPQ 351, 353 (Bd. Pat. App. & Inter. 1984). MPEP§2144.04 VI C.

Applicants contend that neither Yoshioka, Newman, Downey, nor their combinations teaches or discloses each and every feature of the present invention as disclosed in independent claims 1, 11, 19 and 21. As such, the present invention as now claimed is distinguishable and thereby allowable over the rejections raised in the Office Action. The withdrawal of the outstanding prior art rejections is in order, and is respectfully solicited.

Conclusion

In view of all the above, clear and distinct differences as discussed exist between the present invention as now claimed and the prior art references upon which the rejections in the Office Action rely, Applicants respectfully contend that the prior art references cannot anticipate the present invention or render the present invention obvious. Rather, the present invention as a whole is distinguishable, and thereby allowable over the prior art.

Favorable reconsideration of this application is respectfully solicited. Should there be any outstanding issues requiring discussion that would further the prosecution and allowance of

the above-captioned application, the Examiner is invited to contact the Applicants' undersigned representative at the address and phone number indicated below.

Respectfully submitted,

Stanley P. Fisher
Registration Number 24,344

Juan Carlos A. Marquez
Registration Number 34,072

REED SMITH LLP
3110 Fairview Park Drive
Suite 1400
Falls Church, Virginia 22042
(703) 641-4200

June 21, 2004

SPF/JCM/JT